REMARKS

This paper is responsive to the Final Rejection dated March 22, 2006 and the Advisory Action mailed June 14, 2006. Claims 1-61 were examined, all of which were rejected. Claims 62 – 69 have been added. Claims 1, 3, 5, 19, 37, 38, 46, 50, 59, and 61 have been amended. Claims 2, 4, 32 – 36, 39 – 45, 48, and 55 – 58 have been cancelled.

Claims 1-15, 19-49 and 55-60 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,964,867 (hereinafter "Anderson"). Claims 16-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Anderson in view of U.S. Patent Application Pub. No. 2002/0010913 (hereinafter "Ronstrom"). Claims 50-54 and 61 were rejected under 35 U.S.C. §103(a) as being unpatentable over Ronstrom in view of "Efficient Instruction Scheduling Using Finite State Automata" (hereinafter "Bala").

Independent claims 1, 19, 46, and 59 variously recite backtracking a displacement, wherein the displacement is based, at least in part, on a type of operation appropriate for triggering an execution event. Anderson fails to disclose any of the claims. The background of Anderson discloses ***that "all performance counter events...are attributed to the instruction that is executing six cycles after the event."*** *See* col. 3, lines 40 – 49. Hence, the backward analysis steps back an absolute six cycles, which was "a best guess" and is not based on a type of instruction. Anderson does not disclose or suggest the Alpha processor basing the six cycles on a type of operation appropriate for triggering an execution event.

Independent claims 50 and 61 variously recite inserting padding operations to cover at least a portion of an expected detection latency. The Office relies on the background of Ronstrom reference to a European Patent Application publication EP 0 883 059 A2 ("Funama"). Funama discloses inserting a dummy load instruction for a load instruction in code if a longest cache unchanged period is longer than the period between the load instruction and a subsequent consumer of the load instruction. *See* col. 8, line 31 – col. 9, line 23 and Figures 6 and 7. The dummy instruction does not cover expected detection latency. The dummy instruction operates as a prefetch in an attempt to avoid a cache miss. The Office also relies on Bala's disclosure of inserting compensation code. Compensation code discards speculative results if the speculation is incorrect. Inserting speculative operations above a branch and inserting compensation code

does not disclose or suggest inserting padding operations to cover expected detection latency. Neither Funama (via Ronstrom) nor Bala, standing alone or in combination, disclose or suggest inserting padding operation to cover at least a portion of an expected detection latency.

In summary, claims 1, 3, 5 – 31, 37 – 38, 46 – 47, 49 – 54, and 59 – 69 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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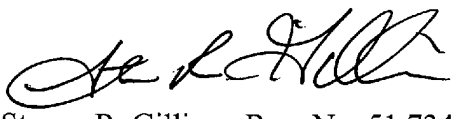

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